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| 10/695,366 | 10/28/2003 | Georg Braun | MUH-12847 | 5189 |

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| EXAMINER | |
|---|---|
| IM, JUNGHWA M | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2811 | |

DATE MAILED: 01/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/695,366 | BRAUN ET AL. | |
| | Examiner | Art Unit | |
| | Junghwa M. Im | 2811 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *02 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-11 and 14-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 14-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/28/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Election/Restrictions*

Applicant's election without traverse of claims 1-11 and 14-19 in the reply filed on November 2, 2005 is acknowledged.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 3 and 16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 3 and 16 recite a unclear limitation of said respective supplying contact device and an associated said respective discharging contact device have a maximum of sixteen different one of said contact devices disposed between them. It is unclear what it means having a maximum of sixteen different one of said contact devices.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-10 and 14-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perino et al. (US 6545875), hereinafter Perino in view of Greeff et al (US 6880082), hereinafter Greeff.

Regarding claim 1, Fig. 11D of Perino shows a memory module for a memory configuration having a bus system with a plurality of signal lines for transmitting data signals, the memory module comprising:

a substrate [three vertical columns];

connection elements [a circular portion on the vertical column] supported by said substrate;

a plurality of memory chips [parts attached by the circular portion] disposed on said substrate and connected to the signal lines through said connection elements; and

contact devices [shadows portions between the substrate].

Fig. 11D of Perino shows most aspect of the instant invention except "contact devices, including supplying contact devices and discharging contact devices, each of the signal lines being connected to a respective one of said supplying contact devices and a respective one of said discharging contact devices, said respective supplying and discharging contact devices associated with one another being disposed physically close together." Fig. 5 of Greeff shows a memory module wherein the contact devices [30] including supplying contact devices [202 in Fig. 3] and discharging contact devices [204 in Fig. 3], each of the signal lines being connected to a respective one of said supplying contact devices and a respective one of said discharging contact devices, said respective supplying and discharging contact devices associated with one another being disposed physically close together. It would have been obvious to one of ordinary skill in the art

at the time of the invention was made to incorporate the teachings of Greeff into the device of Perino in order to have contact devices including supplying contact devices and discharging contact devices, each of the signal lines being connected to a respective one of said supplying contact devices and a respective one of said discharging contact devices, said respective supplying and discharging contact devices associated with one another being disposed physically close together to alleviate the interference in the memory module through having a looped route as taught by Greeff.

Regarding claim 2, Fig. 3 of Greeff shows said contact devices have at least three associated said memory chips, each of said discharging contact devices is disposed at a shorter distance from an associated said respective supplying contact device than, on average, said connection elements associated with the signal line on said memory chips associated with the signal line.

Regarding claim 3, insofar as understood, Fig. 5 of Greeff shows that said contact devices [30] are associated with precisely one of said memory chips [54], and said respective supplying contact device and an associated said respective discharging contact device [in Fig. 3] have a plurality of said contact devices disposed between them.

Regarding claim 4, Fig. 5 of Greeff shows that each respective one of the signal lines is routed essentially without any stub continuously and on a direct path from said respective supplying contact device in succession via said connection elements associated with the respective signal line on said memory chips associated with the respective line to said respective discharging contact device (col. 2, lines 11-24).

Regarding claim 5, Fig. 5 of Greeff shows each respective one of the signal lines is routed essentially without any stub continuously and on a direct path from said respective supplying contact device in succession via said connection elements associated with the respective signal line on said memory chips associated with the respective line to said respective discharging contact device (col. 2, lines 11-24).

Regarding claim 6, Fig. 11D of Perino shows that the contacts [a plug in socket] are disposed in at least one contact row, and in said contact row there is a maximum of two further ones of the contacts devices provided. Therefore, the combined teachings of Perino and Greeff would shows that said contact devices (in lieu of the contact device of Perino) are disposed in at least one contact row, and in said contact row there is a maximum of two further ones of said contact devices provided between each said respective supplying contact device and an associated said respective discharging contact device (Fig. 5 of Greeff shows a detailed configuration of the contact devices as discussed above.)

Regarding claim 7, it is obvious that said memory chips in Fig. 11D of Perino have a chip package with a given length and a given width; and said connection elements associated with a respective signal line are connected to the respective signal line at a respective distance which is obtained from said given length or from said given width of said chip package for said memory chips.

Regarding claim 8, it is obvious that said connection elements [circular portions] in Fig. 11D of Perino have associated with a respective one of the signal lines are connected to the respective signal line substantially at equivalent distances since the connection element are spaced evenly.

Regarding claim 9, Greeff discloses said memory chips each have a double data rate interface (col. 1, lines 50-66).

Regarding claim 10, Fig. 5 of Greeff shows the memory module holds up to 32 [n numbers] of said memory chips for a memory system without error correction devices which contains the memory configuration.

Regarding claim 14, Fig. 11D of Perino shows that said substrate is a rectangular printed circuit board, and said memory chips are disposed in at least two rows in a respective parallel orientation on two opposing surfaces of said rectangular printed circuit board.

Regarding claim 15, the combined teachings of Perino and Greeff fail to show that said rectangular printed circuit board has dimensions 1.7 to 3.0 inches x 5.25 inches. However, it would have been obvious to one of ordinary skill in the art at the time of the invention to have a PCB with a dimension recited in the instant invention to meet a specified package size, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch,* 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 16, insofar as understood, Fig. 11D of Perino shows said contact devices are associated with precisely two of said memory chips, and Fig. 3 of Greeff shows each of said supplying contact devices and an associated said respective discharging contact device have a plurality of said contact devices disposed between them. Therefore, the combined teachings of Perino and Greeff would show that each of said supplying contact devices and an associated said respective discharging contact device have a plurality of said contact devices disposed between them.

Regarding claim 17, Fig. 11D of Perino shows said contact devices have at least three associated ones of said memory chips, and Fig. 3 of Greeff shows each of said discharging contact devices is respectively disposed at a shorter distance from an associated said respective supplying contact device than, an average distance between two memory chips. Therefore, the combined teachings of Perino and Greeff would show that shows said contact devices have at least three associated ones of said memory chips, each of said discharging contact devices is respectively disposed at a shorter distance from an associated said respective supplying contact device than, an average distance between said memory chips.

Regarding claim 18, Fig. 11D of Perino shows a memory configuration for a memory system, the memory configuration comprising:

a system board [10];

a bus system [from the memory chips] having a plurality of signal lines for transmitting data signals and supported by said system board [through being a memory module];

holding devices [a shadowed area holding the substrate; plug in socket on the system board] disposed on said system board;

a bus control chip [11 in Fig. 1] connected to said holding devices; and

memory modules [116] disposed and held by said holding devices, each of said memory modules including:

a substrate [vertical columns on the system board];

connection elements [circular elements on the substrate] supported by said substrate;

a plurality of memory chips [elements on the circular elements] disposed on said substrate and connected to said signal lines through said connection elements; and

contacts [connecting lines formed in the plug in socket].

Fig. 11D of Perino shows most aspect of the instant invention except "contact devices, including supplying contact devices and discharging contact devices, each of the signal lines connected to a respective one of said supplying contact devices and a respective one of said discharging contact devices, said respective supplying contact device and discharging contact device associated with one another being disposed physically close together." Fig. 5 of Greeff shows a memory module wherein the contact devices [30] including supplying contact devices [202 in Fig. 3] and discharging contact devices [204 in Fig. 3], each of the signal lines being connected to a respective one of said supplying contact devices and a respective one of said discharging contact devices, said respective supplying and discharging contact devices associated with one another being disposed physically close together. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Greeff into the device of Perino in order to have contact devices including supplying contact devices and discharging contact devices, each of the signal lines being connected to a respective one of said supplying contact devices and a respective one of said discharging contact devices, said respective supplying and discharging contact devices associated with one another being disposed physically close together to alleviate the interference in the memory module through having a looped route as taught by Greeff.

Regarding claim 19, Fig. 11D of Perino shows said holding devices are precisely four holding devices configured as plug-in sockets.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Perino and Greeff as applied to claim 1 above, and further in view of Seyyedy (US 6282689).

Regarding claim 11, the combied teachings of Perino and Greeff show most aspect of the instant invention the memory module holds up to 36 of said memory chips for except "a memory system with error correction devices which contains the memory configuration." Fig. 3 of Seyyedy shows a memory module with error correction devices which contain the memory configuration. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Seyyedy into the device of Perino and Greeff in order to have a memory system with error correction devices which contains the memory configuration to detect a error in the system.

## *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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